

IN THE SPECIFICATION

**Please replace the paragraph beginning on page 1, line 5, with the following paragraph:**

This application is a continuation application of co-pending U.S. application Serial No. 10/145,122, filed May 15, 2002, <sup>Pat. 6,747,311</sup> which claims the benefit of the earlier filing date of co-pending U.S. Patent application serial number 09/556,777, filed on April 25, 2000, and Japanese Patent Application No. 11-118115, filed April 26, 1999. The entire contents of those applications are incorporated herein by reference.

**Please replace the paragraph beginning on page 5, line 17, with the following paragraph:**

A nonvolatile semiconductor memory device according to an aspect of the invention comprises: a semiconductor substrate having a peripheral circuit region and a memory cell region; a plurality of erasable and programmable memory cell transistors each having a gate electrode and provided in the memory cell region; a plurality of peripheral transistors each having a gate electrode and provided in the peripheral circuit region; first post-oxidation films each provided on the gate electrode of all of the plurality of erasable and programmable memory cell transistors; second post-oxidation films each provided on the gate electrode of all of the plurality of peripheral transistors; first insulating films each provided on the first post-oxidation films and covering a side surface of the gate electrode of all of the plurality of erasable and programmable memory cell transistors, the first insulating films being harder for an oxidizing agent to pass therethrough than a silicon oxide film, and the first insulating films being oxidized; and second insulating films each provided on the second post-oxidation films and covering a side surface of the gate electrode of all of the peripheral transistors, the second